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10/630,647	07/29/2003	Jeffery Steven Beck	MICR-162US	8261

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EXAMINER	
TRAN, NHAN T	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/630,647	BECK ET AL.	
	Examiner	Art Unit	
	Nhan T. Tran	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 May 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 5/21/2007 with respect to claims 1-19 have been considered but are moot in view of the new ground of rejection.

Drawings

2. The replacement drawing of Fig. 3 filed 5/21/2007 is accepted.

Claim Objections

3. Claims 9, 12, 14, 16 & 17 are objected to because of the following informalities:

Regarding claim 9, this claim recites "**the** reset period" in the last phrase of the claim which should be corrected to read as – **a** reset period –.

Regarding claim 12, this claim recites "**the** row trace" in the second line of the claim which should be corrected to read as -- **a** row trace --.

Regarding claim 14, this claim recites "**the** detection" in line 10 of the claim which should be corrected to read as -- detection --, or -- a detection --.

Regarding claim 16, this claim recites "**the** resetting of the light level signal" and "**a** first control node" in lines 6-9 of the claim. These limitations should be corrected to respectively read as -- **resetting** the light level signal -- and -- **the** first control node --.

Regarding claim 17, this claim recites "wherein the:" and "**a** second control node" in lines 1-2 of the claim which should be corrected to respectively read as -- **wherein:** the -- and -- **the** second control node --.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 18 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 18 recites the limitation "the control node" in lines 3-4 of the claim. There is insufficient antecedent basis for this limitation in the claim since there are **two different control nodes** ("a first control node" and "a second control node") in the independent claim 16. It is not clear in claim 18 that which control node the claim is referenced to.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-3, 5-6, 9, 11-12, 14-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Gowda et al. (US 5,877,715).

Regarding claim 1, Gowda discloses a pixel-capture circuit (Fig. 4), comprising:

a pixel-capture device (photodiode 26) having a node (the cathode node of photodiode 26, which is between the photodiode 26 and the row select transistor 22) and operable to convert light intensity into a pixel signal at the node, the pixel signal representing a captured pixel (see Fig. 4; col. 6, lines 59-63 and col. 6, lines 10-13, wherein the pixel signal representing a captured pixel is the photocharge collected at the cathode of the photodiode 26 before transferring the photocharge to the reference node 25);

a row node (a gate node of transistor 22) carrying a row signal (row select signal) that is operable to couple the node (the cathode node of photodiode 26) to a column trace (15j) during a read period (period t4 – t8 shown in Fig. 5 when row select is pulsed to HIGH) of the captured pixel and operable to set the node to a predetermined signal level (VR voltage level) during a reset period (reset period t8 ~ t11 at 66i+1 shown in Fig. 5), wherein the row signal changes between predetermined voltage levels (from HIGH to LOW at t9) during at least one portion (t8 ~ t10) of the reset period (see Figs. 4 & 5 and col. 9, lines 8-22, wherein both the photodiode 26 and reference node 25 are reset to VR during the reset period in which the row select signal is maintained HIGH at t8 and then pulsed to LOW at t9).

Regarding claim 2, Gowda also discloses a reset trace (RESi shown in Fig. 4) carrying a reset signal that is operable to uncouple the node (the cathode node) from **a** row trace (row bus line 34i shown in Figs. 3 & 4 is considered as "**a** row trace" since it is traced in a row direction and not necessarily to be the same as the row select trace RSLi) during the reading the captured pixel (see Fig. 5; col. 9, lines 8-22, wherein the reset signal is set to LOW to uncouple the node from the bus line 34i carrying reset VR voltage during the reading period t4 – t8 to allow the photocharge to accumulate and read out to the column trace 15j properly).

Regarding claim 3, because the image sensor in Gowda is a CMOS image sensor (col. 1, lines 20-24), the pixel-capture device is inherently disposed on a silicon substrate (e.g., a semiconductor substrate).

Regarding claim 5, it is clear in Gowda that the pixel-capture device comprises a photodiode (26 shown in Fig. 4 and col. 6, lines 10-13).

Regarding clam 6, it is also clear in Gowda that the pixel signal comprises a voltage (col. 6, lines 10-13).

Regarding claim 11, Gowda discloses all limitations of claim 11 as analyzed in claim 1 with additional disclosure of CMOS array (Fig. 3 and col. 1, lines 20-24).

Regarding claim 12, this claim is also met by the analysis of claim 2. Note that "the row trace" is objected due to informalities set in section 3 above, and is thus understood as **a** row trace.

Regarding claim 14, Gowda also discloses a system (imaging system shown in Fig. 3) comprising all limitations as analyzed in claims 1 & 11 above. Gowda further discloses a processor (ADC array 40 shown in Fig. 3) coupled with the CMOS array (20) and operable to facilitate detection (by comparator 42j of ADC 40) of a voltage signal at each column trace in each pixel in the CMOS array (see col. 4, lines 46-58, wherein analog voltage output from each pixel on the column trace is detected by the comparator of the ADC 40 so as to convert the analog voltage signal into digital signal).

Regarding claim 15, also shown by Gowda in Fig. 3 is a memory (indicated by "image storage electronics") coupled to the processor and operable to store the pixel signal (col. 5, lines 16-18).

Regarding claim 16, Gowda discloses a method, comprising:

integrating an amount of light (by photodiode 26; Fig. 4 and col. 6, lines 59-63, wherein incident light is integrated by the photodiode by collecting and converting light intensity into photocharge signal);

generating a light level signal on a pixel node (the cathode node of photodiode 26, which is between the photodiode 26 and the row select transistor 22), the pixel node

signal having a level (photocharge level) related to the integrated amount of light (Figs. 4 & 5 and col. 6, lines 59-63, 10-13);

generating a first control signal (row select signal) on a first control node (gate node of row transistor 22 shown in Figs. 4 & 5); generating a second control signal (reset signal) on a second control node (gate node of reset transistor 21) to control resetting of the light level signal (see Figs. 4 & 5 and col. 9, lines 8-22);

reading the light level signal in response to the control signal on [a] *the* first control node (reading period from t4 - t8 in response to row select signal being pulsed to HIGH as shown in Fig. 5; col. 8, lines 18-25 and col. 9, lines 8-10);

resetting the level of the light level signal at the pixel node in response to the second control signal (reset signal) on the first control node (see col. 9, lines 8-22, wherein the resetting effectively resets the photodiode 26 to VR voltage level in the period t8 – t9 where both row select transistor 22 and reset transistor 21 are pulsed to HIGH as shown in Fig. 5, col. 9, lines 8-22), wherein the resetting of the signal level occurs during a reset period (t8 ~ t11) and includes driving the resetting of the level of the light level signal using the first control signal (the row select signal to drive the pixel node to the VR voltage level), the first control signal changing between predetermined levels (changed from HIGH to LOW) during at least one portion (t8 – t10) of the reset period (see Fig. 5 and col. 9, lines 8-22).

Regarding claim 17, as clearly seen in Fig. 5 of Gowda that the reading of the light level signal comprises detecting a level at [a] the second control node (the reset

signal level at the reset gate 21 is always detected by the timing and control logic circuit 14' shown in Fig. 3 by inherency during the reading period from t6 – t8 as shown in Fig. 5, where reset signal level is detected as LOW while the row select signal is HIGH).

Regarding claim 18 *(it is noted that the Examiner's interpretation of this claim is based on best understood in view of the USC 35 112 second paragraph rejection in section 5 above)*, Gowda also discloses that the driving of the resetting of the level of the light level signal comprises: setting a level at the control node (assumed "the second control node") to a predetermined high level (see Fig. 5, wherein the reset signal is pulsed to high level at t8 ~ t11); and pulsing the level at the control node (assumed "the second control node") to a predetermined low level from the predetermined high level (the reset signal is pulsed to low level from the high level at approximate t11 as shown in Fig. 5; see col. 9, lines 8-22).

Regarding claim 19, Gowda further discloses a reset transistor (21 shown in Fig. 4) for controlling the reset of the pixel signal at the node of the pixel capture device (see Figs. 4 & 5 and the analyses of claim 1), the reset transistor being controlled by a reset signal (reset signal on line RESi shown in Figs. 4 & 5) from a reset node (the gate node of reset transistor 21);

a row selection transistor (22 shown in Fig. 4), wherein the row node (the gate node of row select transistor 22) is coupled to the reset transistor (note that the limitation "coupled" is given its broadest reasonable interpretation in which the gate

node of row select transistor 22 is coupled to the reset transistor 21 by timing and control logic 14' shown in Fig. 3 and/or they are coupled together by the physical structure of the pixel circuit as shown in Fig. 4 since the claim does not require how they are coupled, i.e., directly, indirectly, electrically or structurally coupled?) to selectively couple the row node to the node of the pixel capture device for reset (the gate node of transistor 22 is structurally coupled to the cathode of the photodiode 26 via its gate such that the photodiode is reset to VR voltage when the gate node of transistor 22 is pulsed to HIGH at t8 – t9 during the reset period t8 ~ t11 as shown in Fig. 5 and col. 9, lines 8-22) and the row node is further coupled to the row selection transistor (transistor 22) to control the row selection transistor to selectively couple the node of the pixel capture device to a column trace (15j) for readout (during period t4 – t8 as shown in Fig. 5 and col. 9, lines 8-22).

Regarding claim 9, Gowda discloses a pixel-capture circuit (Figs. 3 & 4) comprising:

a pixel-capture device (photodiode 26 shown in Fig. 4) having a first (anode of the photodiode) and second node (cathode of the photodiode), the first node coupled to a first supply node (ground node connected to the anode of the photodiode 26);

a first transistor (transistor 23 shown in Fig. 4) having a control node (gate node of transistor 23), a first drive node (the node connected to bus line 34i carrying VR voltage), and a second drive node (drain node connected to column line 15j), the control

node coupled to the second node (cathode) of the pixel-capture device and the first drive node coupled to a second supply node (VR voltage);

a second transistor (transistor 22 shown in Fig. 4) having a control node (gate node of transistor 22), a first drive node (the node connected to photodiode 26), and a second drive node (node 25), the control node of the second transistor coupled to a row node (row select node), the first drive node of the second transistor coupled to the second drive node of the first transistor, the second drive node of the second transistor coupled to a column node (column node at line 15j) (see Fig. 4 and note that the limitation "coupled" is given its broadest reasonable intepretation since the claim does not require how the nodes are coupled, i.e., directly, indirectly, electrically or structurally coupled? *By definition, "couple" or "coupled" is to connect for consideration together (see online Merriam-Webster dictionary).* Thus, in general, all nodes of the pixel circuit shown in Fig. 4 of Gowda are *at least* structurally coupled together, either directly or indirectly, to form a single integrated circuit as disclosed. Furthermore, during the row select is pulsed to HIGH as shown in Fig. 5, the first node and second node of the second transistor 22 are both coupled to the second node of the first transistor at column line 15j in order to read out photocharge collected by the photodiode 26 as disclosed in col. 8, lines 18-25 and col. 9, lines 8-22);

a third transistor (transistor 21 shown in Fig. 4) having a control node (gate node), a first drive node (node 25), and a second drive node (node connected to bus line 34i carrying VR voltage), the control node of the third transistor coupled to a reset node (reset node at RESi), the first drive node of the third transistor coupled to the row

node (similar to the broadest reasonable intepretation of the limitation "coupled", the node 25 is at least structurally coupled to the row select node), the second drive node of the third transistor coupled to the second node of the of the pixel-capture device (the node at bus line 34i is also structurally coupled to the cathode of the photodiode 26 in view of the broadest reasonable intepretation), wherein the row node carries a row signal (row select signal), the row signal changes between predetermined levels (changed from HIGH to LOW at t9 as shown in Fig. 5) during at least one portion (t8 – t10) of [the] reset period (see col. 9, lines 8-22).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 4, 7-8 & 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gowda (5,877,715) in view of Sasaki (US 6,150,676).

Regarding claim 4, Gowda is silent about that the row trace, the column trace, and the reset trace are disposed within no more than two conductive layers disposed on the silicon substrate.

However, as taught by Sasaki in Figs. 4-6, an image sensor comprises a row trace (row selection line 21), a reset trace (reset line 22) and a column trace (output

signal line 31) being disposed within no more than two conductive layers (a first layer contains lines 21, 22, 23 & 24 and a second layer contains lines 31 & 32 as shown in Fig. 6) disposed on a silicon substrate (60). See Sasaki, col. 6, line 66 – col. 7, line 13. Such wiring layout for the image sensor minimizes the thickness of the image sensor to produce a compact image sensor (Sasaki, col. 4, lines 10-15) while inherently reducing manufacturing cost by minimizing a number of wiring layers.

Therefore, it would have been obvious to one of ordinary skill in the art to combine the teachings of Gowda and Sasaki to layout the row trace, the column trace and the reset trace within no more than two conductive layers disposed on the silicon substrate so as to minimize the thickness of the pixel-capture circuit to produce a compact pixel-capture circuit while reducing manufacturing cost by minimizing a number of wiring layers.

Regarding claim 7, Gowda in view of Sasaki clearly teaches a substrate (see Sasaki, substrate 60 shown in Fig. 5 & 6, col. 7, line 15); two conductive layers disposed on the substrate (see the analysis of claim 4); and one or more conductive paths respectively operable to carry the row signal, each of the conductive paths disposed in a respective one of the two conductive layers (see Sasaki, Figs. 4-6 and note the analysis of claim 4 in which each pixel has at least one row selection line 21 disposed in one of the two conductive layers, and there are plurality of pixels in the image sensor as shown in Fig. 7. Thus, each of a plurality of row selection lines 21 disposed in one of the two conductive layers).

Regarding claim 8, Gowda in view of Sasaki as discussed in claims 4 & 7 also teaches that the pixel capture circuit comprises no conductive layers disposed on the substrate other than the two conductive layers (Sasaki, Figs. 4-6 and col. 6, line 66 – col. 7, line 13 in which only two conductive layers are implemented).

Regarding claim 13, Gowda in view of Sasaki as discussed in claim 4 clearly teaches that a first conductive layer has the row trace (row selection line 21) and the reset trace (reset line 22) disposed therein and a second conductive layer has the column trace (output signal line 31) disposed therein (see Sasaki, Figs. 4-6 and col. 6, line 66 – col. 7, line 13).

7. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gowda (5,877,715) in view of Fossum et al. (US 5,949,483).

Regarding claim 10, Gowda also discloses that the first (23), second (22) and third (23) transistors comprise FET transistors (see Fig. 4; col. 1, lines 20-24 and col. 6, lines 63-67). Gowda does not explicitly disclose that the first, second and third transistors are MOSFET transistors. As taught by Fossum, each of FET transistors in an active CMOS image sensor is preferably implemented with MOSFET for its compatibility with the industry standard CMOS process (see Fossum, col. 8, lines 47-53).

Therefore, it would have been obvious to one of ordinary skill in the art to use MOSFET transistors as the first, second and third transistors in Gowda since MOSFET is preferable for its compatibility with the industry standard CMOS process as taught by Fossum.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (571) 272-7371. The examiner can normally be reached on Monday - Friday, 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

NHAN T. TRAN
Patent Examiner